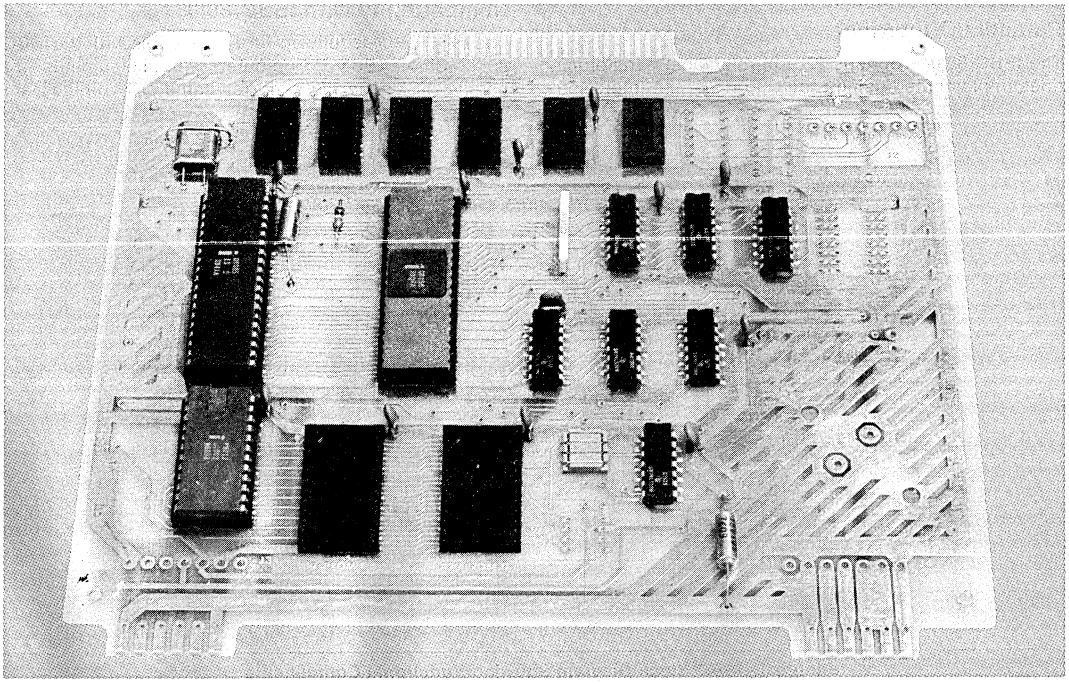
iSBC 80/04
SINGLE BOARD COMPUTER

- 8085A CPU used as central processor
- 256 bytes of static read/write memory
- Sockets for 4K bytes of erasable reprogrammable read only memory
- 22 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators
- Optimized for stand-alone applications with provisions for on-board +5V regulator, heat sink, and mounting holes for attachment to user's equipment
- Programmable 14-bit binary timer
- TTL serial I/O interface with hole patterns for RS232C line drivers and receivers
- Four-level vectored interrupt
- Upward compatibility with iSBC 80/05
- Single +5V power supply

The iSBC 80/04 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. The iSBC 80/04 is a complete computer system on a single 6.75 x 7.85-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial interface, priority interrupt logic, and programmable timer all reside on the board.



FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel 8085A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/04. The 8085A CPU is directly software compatible with the popular intel 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum on-board instruction execution time is 2.03 microseconds. A block diagram of iSBC 80/04 functional components is shown in Figure 1.

Memory Addressing

The 8085A CPU has a 16-bit program counter which allows addressing of up to 65,536 bytes of memory. An external stack, located within any portion of iSBC 80/04 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

The iSBC 80/04 contains 256 bytes of read/write memory using the Intel 8155 RAM/IO/Timer. Two sockets for up to 4K bytes of nonvolatile read only memory are provided on the board. Read only memory may be added in 2K-byte increments using Intel 2716 erasable and electrically reprogrammable ROMs (EPROMs). Optionally, if only 2K bytes are required, read only memory may be added in 1K-byte increments using Intel 2708 EPROMs.

Parallel I/O Interface

The iSBC 80/04 contains 22 programmable parallel I/O lines implemented using the I/O ports of the Intel 8155 RAM/IO/Timer. The system software is used to configure the I/O lines in any combination of unidirectional input or output ports as indicated in Table 1. The I/O interface may, therefore, be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 22 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven, or round cable.

Stand-Alone Applications

The iSBC 80/04 is designed to be a cost-effective solution for applications requiring a self-contained computer on a single board without the need for external memory or I/O options. In order to help minimize power supply cost in small systems, the iSBC 80/04 includes provision for an on-board + 5V regulator allowing unregulated voltage to be connected directly on the board. Regulated DC voltages are applied to the board through two 12-pin edge connectors which mate with flat, woven, or round cables. The iSBC 80/04 also includes pins that will accept MOLEX-type connectors for connection of regulated DC voltages. Mounting holes are provided in the corners of the iSBC 80/04 board which permit direct attachment to the user's equipment, thereby eliminating the need for cardcage and backplane.

Compatibility with iSBC 80/05

The iSBC 80/04 is fully upward compatible with the iSBC 80/05 Single Board Computer. Pin assignments for parallel I/O, serial I/O, and regulated DC voltages are

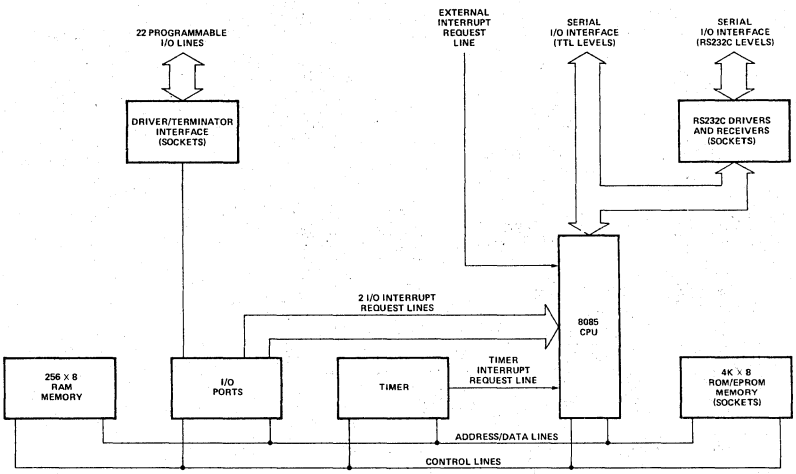


Figure 1. iSBC Block Diagram Showing Functional Components

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation				Control
		Unidirectional				
		Input		Output		
		Unlatched	Latched & Strobed	Latched	Latched & Strobed	
1	8	X	X	X	X	
2	8	X	X	X	X	
3	3	X		X		X[1]
4	3	X		X		X[2]

Notes

1. Port 3 must be used as a control port when port 1 is used as a latched and strobed input or a latched and strobed output port.
2. Port 4 must be used as a control port when port 2 is used as a latched and strobed input or a latched and strobed output port.

indentical to those of the iSBC 80/05. Additionally, software developed for the iSBC 80/04 will execute directly in the iSBC 80/05. In addition to the iSBC 80/04 features, the iSBC 80/05 contains a total of 512 bytes of read/write memory, allows for expansion of memory and I/O capacity, and provides full MULTIBUS arbitration control for multimaster applications.

Programmable Timer

The iSBC 80/04 provides a fully programmable binary 14-bit interval timer utilizing the Intel 8155 RAM/IO/Timer. The systems designer simply configures the time via software to meet system requirements. Whenever a given timer delay is needed, software commands to the programmable timer select the desired functions. Four functions are available as shown in Table 2. The contents of the timer counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Programmable pulse	Timer out goes low during the second half of count. Therefore, the count loaded in the count length register should be twice the pulse width desired.
Square wave rate generator	Timer out remains high until one-half the count has been completed, and goes low for the other half of the count. The count length is automatically reloaded when terminal count is reached.
Rate generator	Divide by N counter. A repetitive timer out low pulse is generated and new timeout initiated every time terminal count is reached.
Programmable strobe	A single low pulse is generated upon reaching terminal count. This function is extremely useful for generation of real-time clocks.

Serial I/O Interface

The iSBC 80/04 prvides serial I/O capability through the serial input data (SID) and serial output data (SOD) functions of the Intel 8085A CPU. These functions are controlled exclusively by software through execution of the 8085A RIM and SIM instructions. The baud rate for the serial I/O interface is determined by the system time available for execution of serial I/O support software. Hence, the maximum baud rate supported by the iSBC 80/04 is solely dependent on the overall system real-time software requirements. Serial I/O signals are TTL compatible, and hole patterns are provided on the board for optional installation of RS232C line drivers and receivers.

Interrupt Capability

The iSBC 80/04 takes advantage of the powerful interrupt processing capability of the 8085A CPU. Interrupt requests are routed to four interrupt inputs of the 8085A CPU (i.e., TRAP, RST 7.5, RST 6.5, and RST 5.5 in order of priority, TRAP highest), and each input generates a unique memory address (i.e., TRAP: 26_{16}, RST 7.5: $3C_{16}$, RST 6.5: 34_{16}, RST 5.5: $2C_{16}$). A single 8085A jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory. All interrupt inputs with the exception of one (TRAP) may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require attention by the 8085A CPU.

Interrupt Generation — The iSBC 80/04 accepts interrupts from four sources. An interrupt is automatically generated by the programmable interval timer/event counter upon completion of the selected function. Two interrupts are automatically generated by the I/O ports section of the 8155 when ports 1 or 2 of the 8155 are programmed to operate in the "latched and strobed" mode (see Table 1). The fourth interrupt source is available to the user and should be used to inform the 8085A CPU of catastrophic errors such as power failure. This user-defined source is connected to the trap input of the 8085A CPU.

Systems Development Capability

The development cycle of the iSBC 80/04-based products may be significantly reduced using an Intellec microcomputer development system. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/04 system software. An optional diskette operating system provides a relocating macroassembler, a relocating loader and linkage editor, and a library manager. A unique in-circuit emulator (ICE-85) option provides the capability of developing and debugging software directly on the iSBC 80/04.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intellec microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

FORTRAN-80 — For applications requiring computational and formatted I/O capabilities, the high level FORTRAN-80 programming language is also available as a resident option of the Intellec system. The FORTRAN compiler produces relocatable object code that may be easily linked with PL/M or assembly language program modules. This gives the user a wide flexibility in developing software.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits
Data — 8 bits

Cycle Time

Basic Instruction Cycle — 2.03 μs, ± 0.1%

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

ROM/EPROM — $0\text{-}0FFF_H$
RAM — $3F00_H$

Memory Capacity

ROM/EPROM — 4K bytes (sockets only)
RAM — 256 bytes

I/O Addressing

On-Board Programming I/O — see Table 1

Port Control	8155 Port 1	8155 Port 2	8155 3 & 4	8155 Ports	8155 Timer Low-Order Byte	8155 Timer High-Order Byte
Address	00	01	02	03	04	05

I/O Capacity

Parallel — 22 programmable lines (see Table 1)

Serial Communications Characteristics

SID and SOD functions of the 8085 CPU are used for serial I/O. Controlled by software through RIM and SIM instructions of the 8085A CPU. Baud rate determined by system time available for serial I/O handling. On-board timer may be used to greatly ease serial I/O timing requirements.

Interrupts

Four-level interrupt routed to 8085 CPU interrupt inputs. Each interrupt automatically vectors the processor to a unique memory location.

Condition	Interrupt Input	Memory Address	Priority	Type
User-defined	TRAP	24_{16}	Highest	Non-maskable
Timer	RST 7.5	$3C_{16}$	↑	Maskable
I/O Port 2	RST 6.5	34_{16}	↓	Maskable
I/O Port 1	RST 5.5	$2C_{16}$	Lowest	Maskable

Timer

Input Frequency Reference — 122.88 kHz ± 0.1% (8.14 μs period nominal)

Output Frequencies/Timing Intervals

Function	Timer/Counter	
	Min	Max
Programmable pulse	8.14 μs	66.67 ms
Square wave rate generator	7.50 Hz	61.44 kHz
Rate generator	7.50 Hz	61.44 kHz
Programmable strobe	8.14 μs	133.33 ms

Interfaces

Parallel I/O — All signals TTL compatible
Interrupt Request — All TTL compatible (active-low)
Serial I/O — TTL; hole patterns available for user installation of RS232C line drivers and receivers

System Clock (8085 CPU)

1.966 MHz ± 0.1%

Connectors

Interface		Pins (no.)	Center (in.)	Mating Connectors[1]
Voltages	+5V, +12V, −5V[2]	7 single-sided	0.156	Molex 09-66-1071 Connector Molex 09-50-7071 Connector
				AMP 87194-6 Connector AMP 3-87025-4 Connector
	+5V, −12V[3]	7 single-sided	0.156	Molex 09-66-1071 Connector Molex 09-50-7071 Connector
				AMP 87194-6 Connector AMP 3-87025-4 Connector
	Unregulated +5V	2 single-sided	0.156	Molex 09-66-1021 Connector Molex 09-50-7021 Connector
				AMP 89194-1 Connector AMP 2-87025-5 Connector
Parallel I/O		50 double-sided	0.1	3M 3415-000 (flat cable)
Serial I/O		7 single-ended	0.156	Molex 09-66-1071 Connector Molex 09-50-7071 Connector
				AMP 87194-6 Connector AMP 3-87025-4 Connector

Notes

1. Connectors and pins from a given vendor may only be used with connectors and pins from the same vendor.
2. A single 86-contact edge-on connector may be used to connect the two groups of regulated voltages (i.e., +5V, +12V, −5V, and +5V, −12V).
3. Required only when RS232C line drivers and receivers are used.

Line Drivers and Terminators

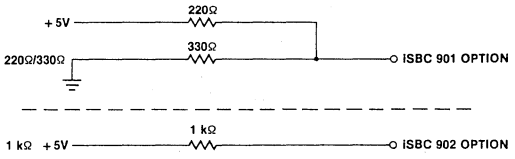
I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/04:

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators — Intel provides 220Ω/330Ω divider and 1 kΩ pull-up resistive terminator packs for termination of I/O lines programmed as inputs. These options are as follows:



RS232C Drivers and Receivers

The following RS232C drivers and receivers are compatible with the RS232C socket on the iSBC 80/04:

RS232C Driver — National DS1488 or TI SN75188
RS232C Receiver — National DS1490 or TI SN75189

Sockets

Sockets may be installed in the hole patterns provided for the RS232C drivers and receivers. The following sockets are compatible with the iSBC 80/04: TI C93-14-02 and SCANBE US-2-14-160-N-B.

Compatible Voltage Regulator

National LM 323 — 3A, 5V Positive Regulator
Fairchild μA7805 KM — 1A, 5V Positive Regulator

Compatible Heat Sink

IERC — LA Series or
AAVID Engineering, Inc. — Series 5051

Physical Characteristics

Width — 7.85 in. (19.94 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 6.0 oz (169.9 gm)

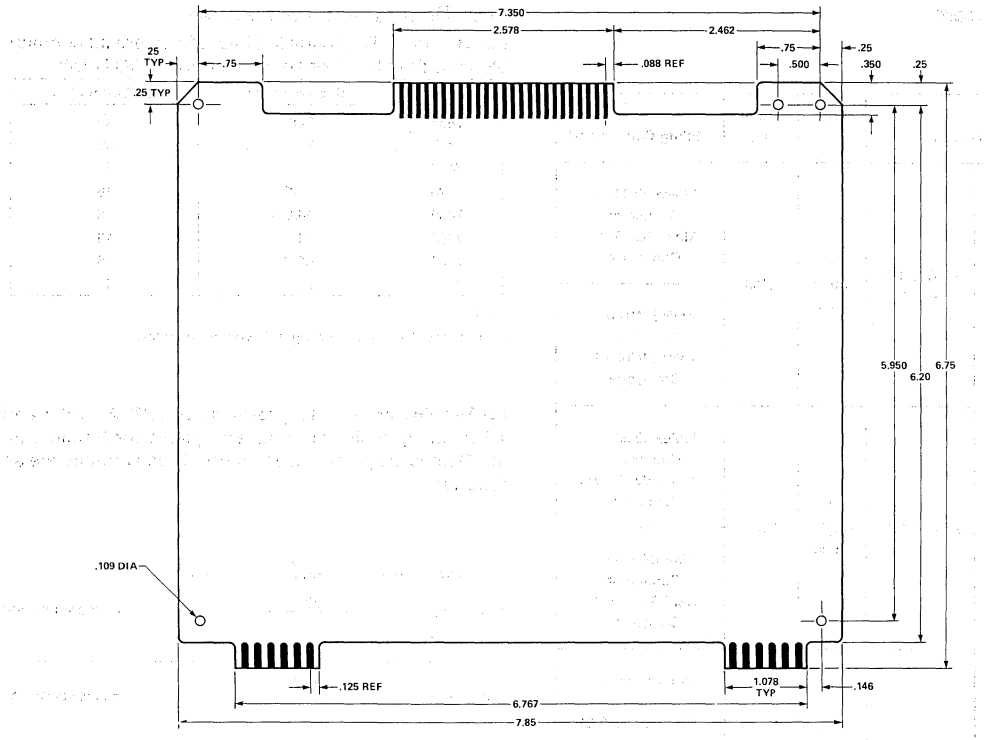


Figure 2. iSBC 80/04 Dimensions

Electrical Characteristics

DC Power Requirements

Voltage (±5%)	Without PROM[1] (max)	With 2716 EPROM[2] (max)	With 2708 EPROM[3] (max)
V_{CC} = +5V	I_{CC} = 600 mA	1.45A	1.25A
V_{DD} = +12V [4]	I_{DD} = 0	7 mA[5]	137 mA
V_{BB} = −5V [4]	I_{BB} = 0	0	90 mA
V_{AA} = −12V [5]	I_{AA} = 0	23 mA[5]	23 mA[5]

Notes

1. Does not include power required for optional EPROM/ROM, I/O drivers, and I/O terminators.
2. With two Intel 2716 EPROMs and 220Ω/330Ω terminators installed for 22 input ports; all terminator inputs low.
3. With two Intel 2708 EPROMs and 220Ω/330Ω terminators installed for 22 input ports; all terminator inputs low.
4. Required for 2708 EPROMs.
5. Required only when RS232C capability required.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manual

9800482-02 - iSBC 80/04 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/04	Single Board Computer