iSBC® 80/16
SINGLE BOARD COMPUTER

The iSBC 80/16 Single Board Computer is a complete computer system that is designed around the 8-bit 8080A-1 MOS microprocessor, clocked at a rate of 2.048 MHz.

The iSBC 80/16 board provides an iSBC 80/10B board replacement for many applications. The board contains 6 JEDEC-compatible memory chip sockets (for installation of up to 64k bytes of user-provided memory), a serial communications port providing an RS232C interface, two parallel I/O ports providing 48 individual I/O lines, two iSBX Bus connectors providing functional expansion by interfacing to all 8-bit iSBX Multimodule boards, and a Multibus interface supporting 8-bit data transfers. The board is shipped with 2k bytes of Static RAM installed into one of the JEDEC-compatible memory sockets.

The iSBC 80/16 board is compatible with the Multibus interface when the board is operated as the only master on the interface, and requires the use of a special Multibus interface control exchange mechanism if used with another bus master. The board receives one interrupt signal from the Multibus interface and is configurable for operation as a limited bus master in a system environment. Compatibility of the iSBC 80/16 board with the iSBC 80/10B board includes compatibility with most of the software designed for the iSBC 80/10B board.

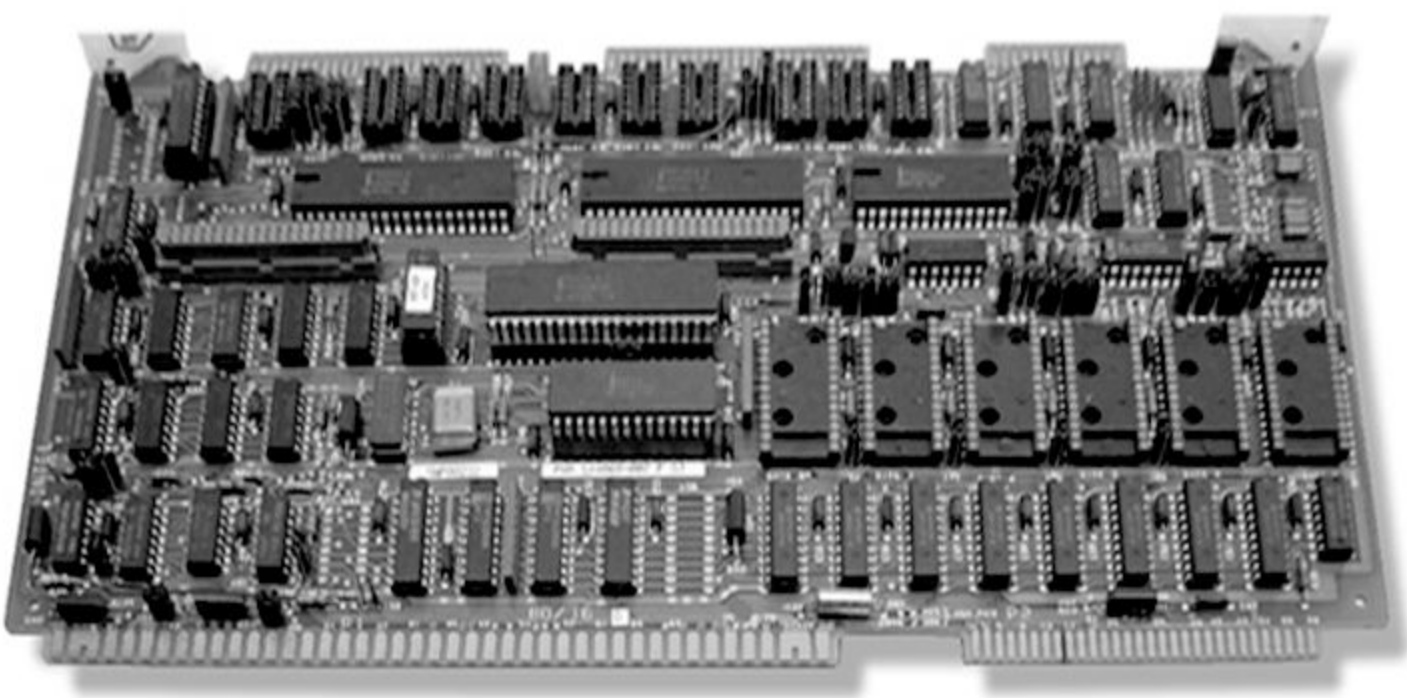

Figure 1-1. iSBC® 80/16 Single Board Computer

1-2. DESCRIPTION

The iSBC 80/16 Single Board Computer, shown in Figure 1-1, is an I/O intensive processor board designed around the 8080A-1 CPU. The iSBC 80/16 board can be configured for compatibility with the software and hardware functions provided by the iSBC 80/10B board, except for the current loop operation, AACK/ support, 2758 EPROM support, and 110 baud operation on the serial interface.

The features of the iSBC 80/16 board are listed in the following text.

* 8080A-1 CPU providing operation at 2.048 MHz clock frequency.
* Software compatible with the iSBC 80/10B Single Board Computer in most applications.
* Six JEDEC-compatible 24/28 pin sockets for installation of up to 64k bytes (maximum) of memory onto the board; 2k bytes of Static RAM is shipped with the board.
* Two iSBX Bus connectors providing interfaces to all 8-bit iSBX Multimodule boards.
* 48 programmable parallel I/O lines on two I/O connectors (J1 and J2) via the 8255A Programmable Peripheral Interface devices.
* 1 interrupt signal from the Multibus interface via the EXT INTR1/ signal line.
* 1 serial RS232C-compatible I/O port provided via the 8251A Programmable Communications Interface device.
* Multibus interface compatibility.

The 8080A-1 CPU is a 40-pin LSI device providing an interface with 8-bit systems. The 8080A-1 CPU contains six 8-bit general purpose registers. The 8-bit registers may be addressed individually or in pairs, providing both single and double precision operators. The 8080A-1 CPU supports a wide range of addressing modes and data transfer operations, and logical operations. The architecture of the 8080A-1 CPU allows you to control the address and data busses via the HOLD signal, a derivitive of the Bus Priority In signal (BPRN/) on the Multibus interface.

Two iSBX Bus interfaces are available on the iSBC 80/16 board via the J4 and J5 connectors. The iSBX Bus connectors allow expansion of the functionality of the iSBC 80/16 board in small increments by installing Multimodule boards such as the iSBX 311 Analog Input Multimodule Board, the iSBX 328 Analog Output Multimodule Board, the iSBX 350 Parallel I/O Multimodule Board, the iSBX 351 Serial I/O Multimodule Board, the iSBX 331 Fixed/Floating Point Math Multimodule Board, the iSBX 332 Floating Point Math Multimodule Board, and others. Each iSBX Bus connector is capable of interfacing to only 8-bit iSBX Multimodule boards.

The iSBC 80/16 board can hold a maximum of 64k bytes of memory in six JEDEC-compatible memory sockets. The six 24/28 pin IC sockets accommodate user-installation of read only memory, electrically erasable memory, or static RAM devices. The sockets may be filled with different memory components in three independent sets of two sockets. Configuration jumpers allow memory device size increments of 2k, 4k, 8k, or 16k bytes.

The iSBC 80/16 board includes 48 programmable parallel I/O lines implemented by means of two Intel 8255A-5 Programmable Peripheral Interface (PPI) devices. The I/O signals are jumper selectable to many combinations of unidirectional input/output and bidirectional ports. The I/O interface may be customized to meet specific peripheral requirements and, in order to take full advantage of the large number of possible I/O configurations, IC sockets are provided for installation of user-supplied I/O line drivers and terminators. This further enhances the flexibility of the parallel I/O interface by allowing combinations of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are available at two 50-pin edge connectors (J1 and J2).

The RS232C-compatible serial I/O port at connector J3 is controlled and interfaced by an Intel 8251A Programmable Communications Interface (PCI) device. Integrated circuits U13 and U14 on the iSBC 80/16 board provide the serial RS232C interface termination for the J3 interface. The PCI is individually programmable for operation in synchronous or asynchronous data transmission modes.

In the synchronous mode the following features are programmable:

a. Character length,
b. Sync character (or characters), and
c. Parity.

In the asynchronous mode the following features are programmable:

a. Character length,
b. Baud rate factor (clock divide ratios of 1, 16, or 64),
c. Stop bits, and
d. Parity.

In both the synchronous and asynchronous modes, the serial I/O port features half- or full-duplex, double buffered transmit and receive capability on an RS232C compatible interface. In addition, PCI error detection circuits can check for parity, overrun, and framing errors. The PCI transmit and receive clock rates are supplied by a jumper selectable baud rate generator. These clocks may optionally be supplied from an external source. The RS232C command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector (J3).

Multibus interface control requests from another bus master are sensed in the iSBC 80/16 board via the Bus Priority In (BPRN/) signal. The jumper-configured signal can suspend 8080A-1 CPU operation while the other master accesses the Multibus interface resources. Note that this bus exchange timing on the iSBC 80/16 board is not compatible with the requirements described in the INTEL MULTIBUS SPECIFICATION (see Figure 2-10).

1-3. SYSTEM SOFTWARE DEVELOPMENT

The development cycle of iSBC 80/16 Single Board Computer based products may be significantly reduced using an Intel Intellec Series II Microcomputer Development System (MDS) with an ISIS-II software package. The ISIS-II Software package includes the high level programming language PL/M 80. PL/M 80 allows programming in a natural, algorithmic language and eliminates the need to manage register usage or memory allocation. The programs can be written in a much shorter time than Assembly Language programs for a given application.

Program development may be performed on the Intel Personal Development System (iPDS) products, however, the iPDS products do not provide the ability to emulate as does the MDS.

1-4. EQUIPMENT SUPPLIED

Each iSBC 80/16 board is shipped with a current revision of the schematic diagram for the board. Insert the current revision drawing into this manual. No other equipment is provided with the iSBC 80/16 board.

1-5. EQUIPMENT REQUIRED

A list of components required to configure the iSBC 80/16 board is provided in Chapter 2. Because the iSBC 80/16 board is designed to satisfy a variety of applications, the user must purchase and install only those components required to satisfy his particular needs.

1-6. SPECIFICATIONS

Specifications of the iSBC 80/16 Single Board Computer are listed in Table 1-1.

Table 1-1. Specifications

CPU	Intel 8080A-1
WORD SIZE	
Instruction:	8, 16, or 24 bits.
Data:	8 bits.
Address:	16 bits.
SYSTEM CLOCK SPEED:	2.048 MHz ±0.1%
INSTRUCTION CYCLE TIME	
At 2.048 MHz:	1950 nanoseconds.
MEMORY ARRAY	
On-board Memory:	6 JEDEC-compatible chip sockets hold user-provided memory devices in 1kx8, 2kx8, 4kx8, 8kx8, 16kx8, or 32kx8 capacity. Sockets must be configured in pairs; 3 independent pairs possible. Note: Installation of 1kx8 and 32kx8 devices requires programming a decode PROM. Refer to Table 2-5 for a list of devices supported by the decode PROM in the as-shipped configuration.
On-board Static RAM:	JEDEC-compatible Static RAM devices; either 2kx8 or 8kx8. One 2k by 8 Static RAM is provided in socket U45. Refer to paragraph 2-12 for more information.
On-board E^2PROM:	JEDEC-compatible E^2PROM devices in socket pair U43/U44 and/or U45/U46. Refer to paragraph 2-12 for more information.
MAXIMUM MEMORY ADDRESS RANGE	64k bytes; 0000 to FFFFH. Addresses at each JEDEC-compatible memory socket depends on the type of decode PROM operation selected.
I/O CAPABILITY	
Parallel:	48 programmable I/O lines using two 8255A PPI devices and parallel I/O connectors J1 and J2.
Serial:	1 programmable RS232C-compatible interface using the 8251A PCI device.
Expansion:	2 iSBX Bus connectors providing expansion via either single-wide or double-wide 8-bit iSBX Multimodule boards.

Table 1-1. Specifications (continued)

SERIAL COMMUNICATIONS CHARACTERISTICS

Synchronous:	5 to 8 bit characters; internal or external character synchronization; automatic sync bit insertion.
Asynchronous:	5 to 8 bit characters; break character generation; 1, 1 1/2, or 2 stop bits; false start-up detection.

Baud Rates:

Output Frequency (in kHz)	Baud Rates		
	Sync Mode (x1)	Asynchronous Mode (x16)	(x64)
307.2	---	19200	4800
153.6	---	9600	2400
76.8	---	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
460.8	---	---	7200
230.4	---	14400	3600
115.2	---	7200	1800
57.6	---	3600	900
28.8	28800	1800	450
14.4	14400	900	225
7.2	7200	450	112.5

PHYSICAL CHARACTERISTICS

Width:	30.48 cm. (12.00 in.)
Length:	17.15 cm. (6.75 in.)
Thickness:	1.27 cm. (0.50 in.)
Weight:	371 gm. (13.0 oz.)

Table 1-1. Specifications (continued)

ENVIRONMENTAL REQUIREMENTS

Operating Temperature:	0°C to 55°C
Relative Humidity:	to 90%, non-condensing

ELECTRICAL CHARACTERISTICS

DC Power Requirements:

	+5V	+12V	-5V[2]	-12V
	(All voltages +/- 5%)			
iSBC 80/16 board [1] Without memory devices	Icc=1.95A	Idd=160mA	Ibb=0mA	Iaa=100mA

Notes: 1. Excludes power requirements for byte-wide devices, I/O driver/terminator devices, and iSBX Multimodule boards.
2. The Vbb power is required only when using 2708 EPROM devices.