SBC 104/108/116 COMBINATION MEMORY AND I/O EXPANSION BOARDS

4K, 8K, 16K bytes of read/write memory (SBC 104, SBC 108, SBC 116, respectively)

Sockets for 4K bytes of programmable or masked read-only-memory

Auxiliary power bus and memory protect control logic provided for battery back-up RAM requirements

48 programmable I/O lines with sockets for interchangeable line drivers and terminators

Synchronous/Asynchronous communications interface with RS232C drivers and receivers

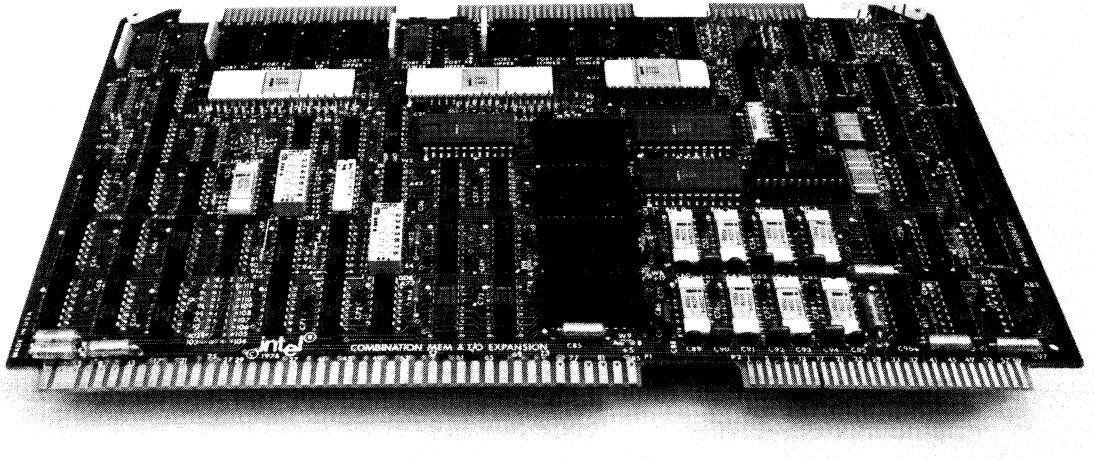
Eight maskable interrupt request lines with a pending interrupt register

1 ms interval timer

The SBC 104, SBC 108, and SBC 116 are members of Intel's complete line of SBC 80 memory and I/O expansion boards. Each board interfaces directly with any SBC 80 Single Board Computer, via the system bus, to expand RAM and ROM memory capacity; serial and parallel I/O capacity.

The SBC 104 contains 4K, the SBC 108 8K, and the SBC 116 16K bytes of RAM memory implemented using Intel dynamic RAM memory components. On-board refresh hardware refreshes a portion of all eight RAM memory elements every 14 microseconds. If a read or write cycle is already in progress when a refresh cycle is scheduled to begin, the refresh cycle is postponed until the end of the read or write cycle. Each refresh cycle utilizes memory for 590 nanoseconds. Typical RAM access time is 485 nanoseconds. Typical Read/Write cycle time is 560 nanoseconds.

Sockets for up to 4K bytes of non-volatile read-only memory reside on the boards. Read-only-memory may be added in 1K byte increments using Intel® 8708 Erasable and Electrically Reprogrammable ROMs (EPROMs) or Intel® 8308 Masked ROMs. Typical ROM/EPROM access time is 440 nanoseconds. Typical ROM/EPROM cycle time is 560 nanoseconds.



MICRO-COMPUTER SYSTEMS

Each combination board contains 48 programmable I/O lines implemented using two Intel® 8255 Programmable Peripheral Interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output, and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, round, or woven cable.

Typical I/O Read access time is 280 nanoseconds. Typical I/O Read cycle time is 600 nanoseconds.

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on each board. A jumper-selectable baud rate generator provides the USART with all common communications frequecies between 75 Hz and 38.4 kHz. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and asynchronous serial transmission rate are all under program control. The 8251 provides full duplex, double-buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of a comprehensive RS232C interface on the boards in conjunction with the USART provides a direct interface to CRTs, RS232C compatible casettes, asynchronous and synchronous modems. The RS232C, serial data lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cables.

The SBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The SBC 530 may be used to interface the SBC 104/108/116 Combination Boards to teletypewriters and other 20 mA current loop equipment.

Interrupt requests may originate from eight sources. Four jumper-selectable interrupt requests can be automatically generated by the Programmable Peripheral Interfaces when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Two jumper-selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). These six interrupt request lines are all maskable under program control. Two interrupt request lines may be interfaced directly from user-designated peripheral devices via the I/O edge connector. An on-board register contains the status of all eight interrupt request lines, and may be interrogated by the CPU. Each interrupt request line is maskable under program control. Routing for the eight interrupt request lines is jumper-selectable. They may be ORed to provide a single interrupt request line for the SBC 80/10, or they may be individually provided to the system bus for use by the SBC 80/20 Priority Interrupt Controller.

Each board contains a jumper-selectable 1 ms interval timer. The timer is enabled by jumpering one of the interrupt request lines from the I/O edge connector to a 1 ms interval interrupt request signal originating from the baud rate generator.

TABLE 1

INPUT/OUTPUT PORT MODES OF OPERATION

PORT	NO. OF LINES	MODE OF OPERATION					
		UNIDIRECTIONAL				BIDIRECTIONAL	CONTROL
		INPUT		OUTPUT			
		UNLATCHED	LATCHED & STROBED	LATCHED	LATCHED & STROBED		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X[2]
	4	X		X			X[2]

NOTES: 1. Part of Port 3 must be used as a control port when either Port 1 or Port 2 are used as a latched and strobed input or a latched and strobed output or Port 1 is used as a bidirectional port.

2. Part of Port 6 must be used as a control port when either Port 4 or Port 5 are used as a latched and strobed input or a latched and strobed output or Port 4 is used as a bidirectional port.

SPECIFICATIONS

MEMORY ADDRESSING

ROM/EPROM

4K segments starting at any jumper-selectable base address on a 4K byte boundary (e.g., 0000_H, 1000_H, ... $F000_H$)

RAM:

4K, 8K, 16K segments starting at any jumper-selectable base address on a 4K byte boundary (e.g., 0000_H, 1000_H, ... $F000_H$)[3]

Note: 3. Base address 7000_H not allowed for SBC 108. Base address $5000_H \rightarrow 7000_H$ not allowed for SBC 116.

MEMORY CAPACITY

ROM/PROM: 4K bytes (sockets only)
RAM: 4K bytes for SBC 104, 8K bytes for SBC 108, 16K bytes for SBC 116.

MEMORY RESPONSE TIME

Memory	Access (ns)	Cycle (ns)
RAM	575 max*	675 max*
EPROM/ROM	465 max	685 max

*Without Refresh Interruption.

I/O ADDRESSING

Port	1	2	3	4	5	6	8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
Address	X4	X5	X6	X8	X9	XA	X7	XB	XC	XD

Note: X is any hex digit assigned by jumper selection.

I/O TRANSFER RATE

Parallel: Read or Write cycle time 760 ns max
Serial: (USART)

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

SERIAL COMMUNICATIONS CHARACTERISTICS

Synchronous:
- 5–8 bit characters
- Internal or external character synchronization
- Automatic Sync Insertion

Asynchronous:
- 5–8 bit characters
- Break characters generation
- 1, 1½, or 2 stop bits
- False start bit detectors

INTERRUPTS

Eight interrupt request lines may originate from the Programmable Peripheral Interface (4 lines), the USART (2 lines) or user specified devices via the I/O edge connector (2 lines) or Interval Timer.

INTERRUPT REGISTER ADDRESSES

Interrupt Mask Register	X1
Interrupt Status Register	X0

Note: X is any hex digit assigned by jumper selection.

TIMER INTERVAL

1.003 ms ±0.1% when 110 Baud Rate is selected
1.042 ms ±0.1% for all other Baud Rates

INTERFACES

Bus: All signals TTL compatible
Parallel I/O: All signals TTL compatible
Serial I/O: RS232C
Interrupt Requests: All TTL compatible

CONNECTORS

Interface	No. of Pins	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Aux Power[4]	60	0.1	AMP PE5-14559 or TI H311130

Note: 4. Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM or MDS packaging.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm) Depth: 0.50 in. (1.27 cm)
Height: 6.75 in. (17.15 cm) Weight: 14 oz (397.3 gm)

ELECTRICAL CHARACTERISTICS[5]

Average DC Current:

		Without EPROM[6]	With EPROM[7]	RAM[8]
V_{CC} = +5V ±5%	I_{CC} = 2.85A max	3.6A max	600 mA max
V_{DD} = +12V ±5%	I_{DD} = 450 mA max	700 mA max	400 mA max
V_{BB} = –5V ±5%	I_{BB} = 3 mA max	180 mA max	3 mA max
V_{AA} = –12V ±5%	I_{AA} = 60 mA max	60 mA max	Not Used

Notes:
5. All current values given here include RAM power.
6. Does not include power required for optional EPROM, I/O drivers, and I/O terminators.
7. With four 8708 EPROMs and eight 220Ω/330Ω Input terminators installed, all terminator inputs low.
8. RAM chips and RAM control logic (powered via Auxiliary Power Bus).

AUXILIARY POWER

An Auxiliary Power Bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this Auxiliary RAM Power Bus is made via jumpers on the board.

MEMORY PROTECT

An active-low TTL compatible MEMORY PROTECT signal is brought out on the Auxiliary connector which, when asserted, disables Read/Write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

LINE DRIVERS AND TERMINATORS

I/O Drivers:

The following line drivers and terminators are all compatible with the I/O driver sockets on the SBC 104/108/116.

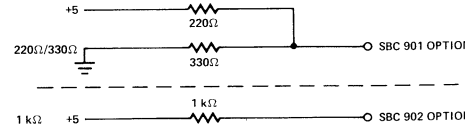
Driver	Characteristic	Sink Current (mA)	Driver	Characteristic	Sink Current (mA)
7438	I,OC	48	7409	NI,OC	16
7437	I	48	7408	NI	16
7432	NI	16	7403	I,OC	16
7426	I,OC	16	7400	I	16

Note: I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 25 mA totem-pole drivers and 1 kΩ terminators.

I/O Terminators:

Terminators: 220Ω/330Ω divider or 1 kΩ pull-up.

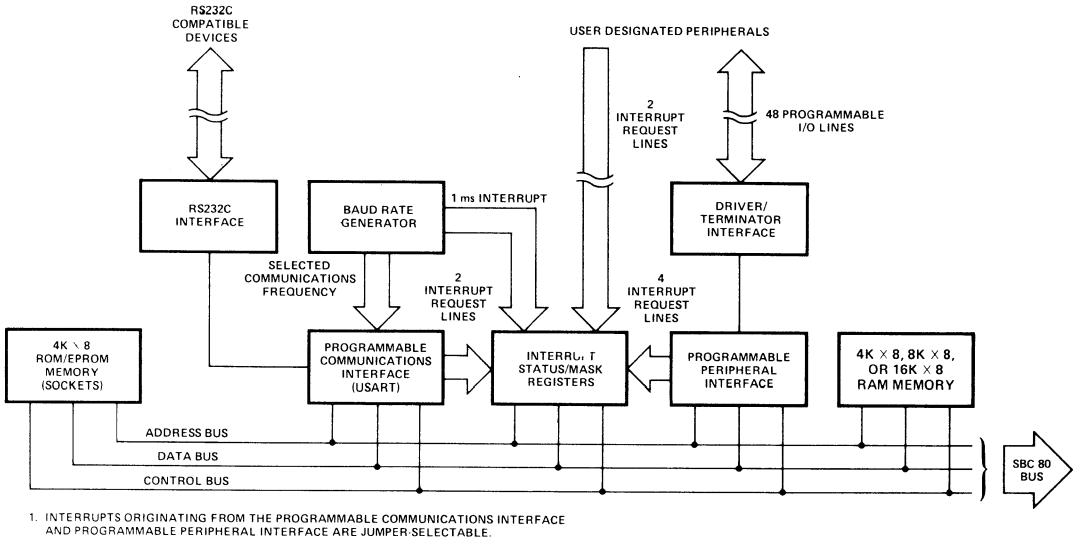


Bus Drivers:

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Commands	Tri-State	25

ENVIRONMENTAL

Operating Temperature: 0°C to +55°C.



1. INTERRUPTS ORIGINATING FROM THE PROGRAMMABLE COMMUNICATIONS INTERFACE AND PROGRAMMABLE PERIPHERAL INTERFACE ARE JUMPER-SELECTABLE.

SBC 104/108/116 BLOCK DIAGRAM